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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,610	12/29/2000	William A. Harris	H16-26054 US	8597

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EXAMINER

COX, CASSANDRA F

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/751,610

Applicant(s)

HARRIS, WILLIAM A.

Examiner

Cassandra Cox

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 11, 12, 14-17 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3 is/are allowed.
- 6) ☒ Claim(s) 4-9, 11, 12, 14-17 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 04 March 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

3. Claims 4-9, 11-12, 14-17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Li et al. (U.S. Patent No. 5,058,132).

In reference to claim 11, Li discloses in Figure 2, a circuit (100) for generating multiphase clock signals, the circuit comprising: a clock generator (the clock generator is seen to be the oscillator 120; column 4, line 65 - column 5, line 15) for generating a first clock at a clock frequency F_0 ; a phase lock loop circuit (102) receiving the first clock signal (116) and providing an output signal (124); and a Johnson counter (114) having N stages connected to receive as an input the output signal (124) of the phase lock loop circuit (102) and providing an output signal (LBC1-5) as an error signal to the phase lock loop circuit (column 5, lines 25-28); the Johnson counter (114) also connected for providing output signals (LBC1-LBC5) from each of the N stages of the Johnson counter (114) as further clock signals, wherein the output signals being phase shifted from the first clock signal by a fixed angular increment is seen to be inherent feature of the outputs of counters. The same applies to claims 4-5, wherein the multistage counting

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circuit is seen to be the Johnson counter (114) and the clock generator is seen to be the oscillator (120; column 4, line 65- column 5, line 15).

In reference to claim 12, the output signal of the phase lock loop circuit has a frequency of $2NF_0$.

In reference to claim 6, Li discloses in Figure 2, a circuit for receiving an input clock signal (116) and generating a plurality of clock signals (LBC1-LBC5) having frequencies identical to the input clock signal (116) and predetermined phase displacements from the input signal, comprising: a phase detector (104) for comparing an input clock signal (116) to a feedback signal (123) and providing an output signal (121) corresponding to the phase difference between the input clock signal (116) and the feedback signal (123); a low pass filter and gain stage (106) receiving the output signal from the phase comparator (104) and producing a control signal (125); a voltage controlled oscillator (108) for receiving the control signal and producing an oscillator output signal (124) having a frequency corresponding to the control signal (125); and a multistage counting circuit (114) connected to receive the oscillator output signal (124) and provide the feedback signal (123; column 5, lines 50-67) to the phase detector (104) and a plurality of clock signals (LBC1-LBC5) at the frequency of the input clock signal (116) and phase shifted from the clock signal by fixed angular increments, wherein the output signals being phase shifted from the first clock signal by fixed angular increments is seen to be an inherent feature of the outputs of counters. The same applies to claims 7, 14, and 16.

In reference to claim 8, Li also discloses in column 5, lines 1-22 that the frequency (125MHz) of the voltage controlled oscillator output signal (124) is a multiple of the frequency (12.5 MHz) of the input clock signal (116). The same applies to claims 17, and 19.

In reference to claim 9, Li also discloses in Figure 2 that the multistage counting circuit (114) is a Johnson counter having N stages. The same applies to claim 15.

4. Claims 4-9, 11, 14-17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii (U.S. Patent No. 5,315,269).

In reference to claim 6, Fujii discloses in Figure 7, a circuit for receiving an input clock signal (61-64) and generating a plurality of clock signals (71-74) having frequencies identical to the input clock signal (61-64) and predetermined phase displacements from the input signal, comprising: a phase detector (11-14) for comparing an input clock signal (61-64) to a feedback signal (71-74) and providing an output signal (OUT) corresponding to the phase difference between the input clock signal (61-64) and the feedback signal (71-74); a low pass filter and gain stage (102) receiving the output signal from the phase comparator (11-14) and producing a control signal; a voltage controlled oscillator (VCO) for receiving the control signal and producing an oscillator output signal (OUT) having a frequency corresponding to the control signal; and a multistage counting circuit (105, shown in Figure 8) connected to receive the oscillator output signal (OUT) and provide the feedback signal (71-74) to the phase detector (11-14) and a plurality of clock signals (71-74) at the frequency of the input clock signal (61-64) and phase shifted from the clock signal by fixed angular increments, wherein the

output signals being phase shifted from the first clock signal by fixed angular increments is seen to be an inherent feature of the outputs of counters. The same applies to claims 7, 14, and 16.

In reference to claim 8, Fujii also discloses in column 4, lines 3-8 that the frequency ($\pm 2N\pi$) of the voltage controlled oscillator output signal (OUT) is a multiple of the frequency ($\pm 2\pi$) of the input clock signal (116). The same applies to claims 17 and 19.

In reference to claim 9, Fujii also discloses in Figure 8, column 5, and lines 1-16 that the multistage counting circuit (105) is a Johnson counter having N stages. The same applies to claim 15.

In reference to claim 11, Fujii discloses in Figure 5, a circuit for generating multiphase clock signals, the circuit comprising: a clock generator (104) for generating a first clock at a clock frequency F_0 ; a phase lock loop circuit (101, 102, 103) receiving the first clock signal (output of 104) and providing an output signal (OUT); and a Johnson counter (105; see column 5, lines 1-2 and 14-16) having N stages connected to receive as an input the output signal (OUT) of the phase lock loop circuit (101, 102, 103) and providing an output signal as an error signal to the phase lock loop circuit (column 3, lines 60-63); the Johnson counter (105) also connected for providing output signals (shown in Figure 8) from each of the N stages of the Johnson counter (105) as further clock signals, wherein the output signals being phase shifted from the first clock signal by a fixed angular increment is seen to be an inherent feature of the outputs of counters. The same applies to claims 4-5, wherein the multistage counting circuit is

seen to be the Johnson counter (114) and the clock generator is seen to be the oscillator (120; column 4, line 65- column 5, line 15).

Response to Arguments

5. In response to applicant's argument with respect to claims 4-9, 11-12, 14-17, and 19, the previous indication of allowability of claims 6-9 has been withdrawn; therefore applicant's arguments are moot. Upon further review of the claimed invention, the examiner finds that the outputs of counter stages are inherently displaced from the input signal by a fixed angle. This action is Non-Final.

Allowable Subject Matter

6. Claims 1-3 are allowed.

7. The following is an examiner's statement of reasons for allowance: Claims 1-3 and 20-21 are allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the clock signals each have a phase displaced from the phase of the other by $360^\circ/2N$ in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
August 27, 2002

Kenneth B. Wells
Kenneth B. Wells
Primary Examiner